

Examination (SS 2021)

Communication Systems and Protocols

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Exam: Communication Systems and Protocols

Date: July 27, 2021

Participant:

Matr. No.:

ID:

Lecture hall:

Seat No.:

The following rules apply:

- The writing time of the examination is 120 minutes.
- No examination aids are permitted, except for
 - a DIN-A4 sheet of hand-written notes,
 - a non-programmable calculator, and
 - a dictionary.
- Use only **document-proof writing instruments** and no red ink.
 - Pencils and correction fluid, for example, are not document-proof.
- You are not permitted to use your own writing paper.
- Please do not write on the back sides of the sheets.
- Additional solution sheets are available from the examination supervisors.
 - Make sure that you label all such sheets with your matriculation number.
 - Each additional solution sheet needs to be assigned to exactly one task.

The examination comprises **35 sheets**.

Task	Points	Score
1	32	
2	30	
3	31	
4	30	
5	30	
6	27	
7	31	
8	31	
Σ	242	

Task 1: Physical Basics

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Sampling and A/D conversion

1.1 Name the four classes of signals which exist in communication channels.

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An exemplary signal is shown below.

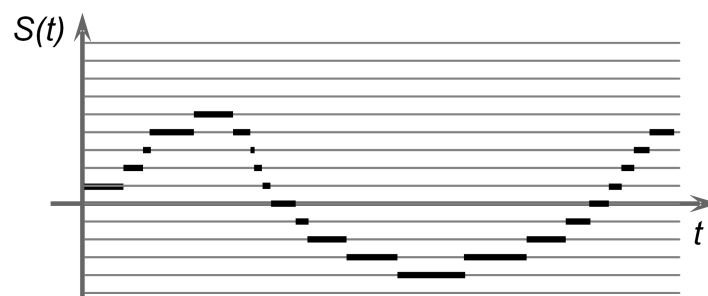


Figure 1.1: Exemplary signal

1.2 Which class does the signal shown in Figure 1.1 belong to?

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When integrating an AD converter, a sample & hold gate is needed. An exemplary sample & hold gate is given in Figure 1.2.

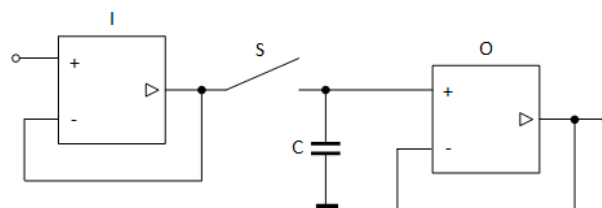


Figure 1.2: Sample & hold gate

1.3 What is the purpose of the sample & hold gate for the AD conversion process?

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- 1.4 Briefly describe the purpose of every subblock (I, O, S, C) of the sample & hold gate. What is its function inside the sample & hold gate?

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Channel capacity

A digital baseband transmission system has a maximum frequency of 30 kHz.

- 1.5 Assuming an ideal channel, calculate the maximum data rate achievable on this channel using ternary signals?

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- 1.6 Which problem arises when we keep increasing the number of signal steps in a real channel to achieve a higher data rate?

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Reflection on wires

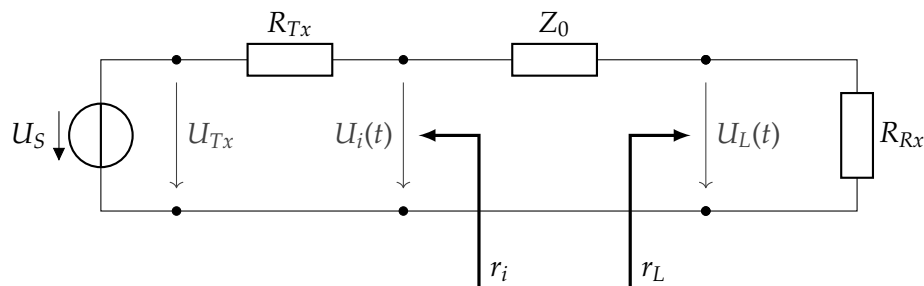


Figure 1.3: Test setup

Figure 1.3 shows the equivalent circuit diagram of an ideal (lossless) transmission line: A transmitter having output impedance R_{Tx} is connected to a receiver with the input impedance R_{Rx} using a long cable.

$R_{Tx} = 60 \Omega$ and $R_{Rx} = 180 \Omega$. The signal line is characterized by $Z_0 = 60 \Omega$.

- 1.7 Give the generic formula to calculate the reflection factor and give the reflection factors r_i and r_L .

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At the time $t = 0$ the voltage U_S of the sender changes from 0 V to 5 V and is constant afterwards. The run time of a wave on the cable is t_d .

- 1.8 Calculate the value of the voltage $U_i(t)$ at the time $t = 0$.

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1.9 Calculate the voltage $U_m(t)$ in the middle of the line at the times $t \in \{0, t_d, 2t_d, 3t_d\}$. Neglect all transient events, use ideal rectangular impulses for calculation.

Task 2: Transmission Principles

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Line Codes

2.1 The value **1101 1001 0101** shall be transmitted through a serial wire communication channel. Complete Figure 2.1 with the digital signals transmitted using each given encoding scheme. All codes start from their lower state (-Level 1 or Level 2).

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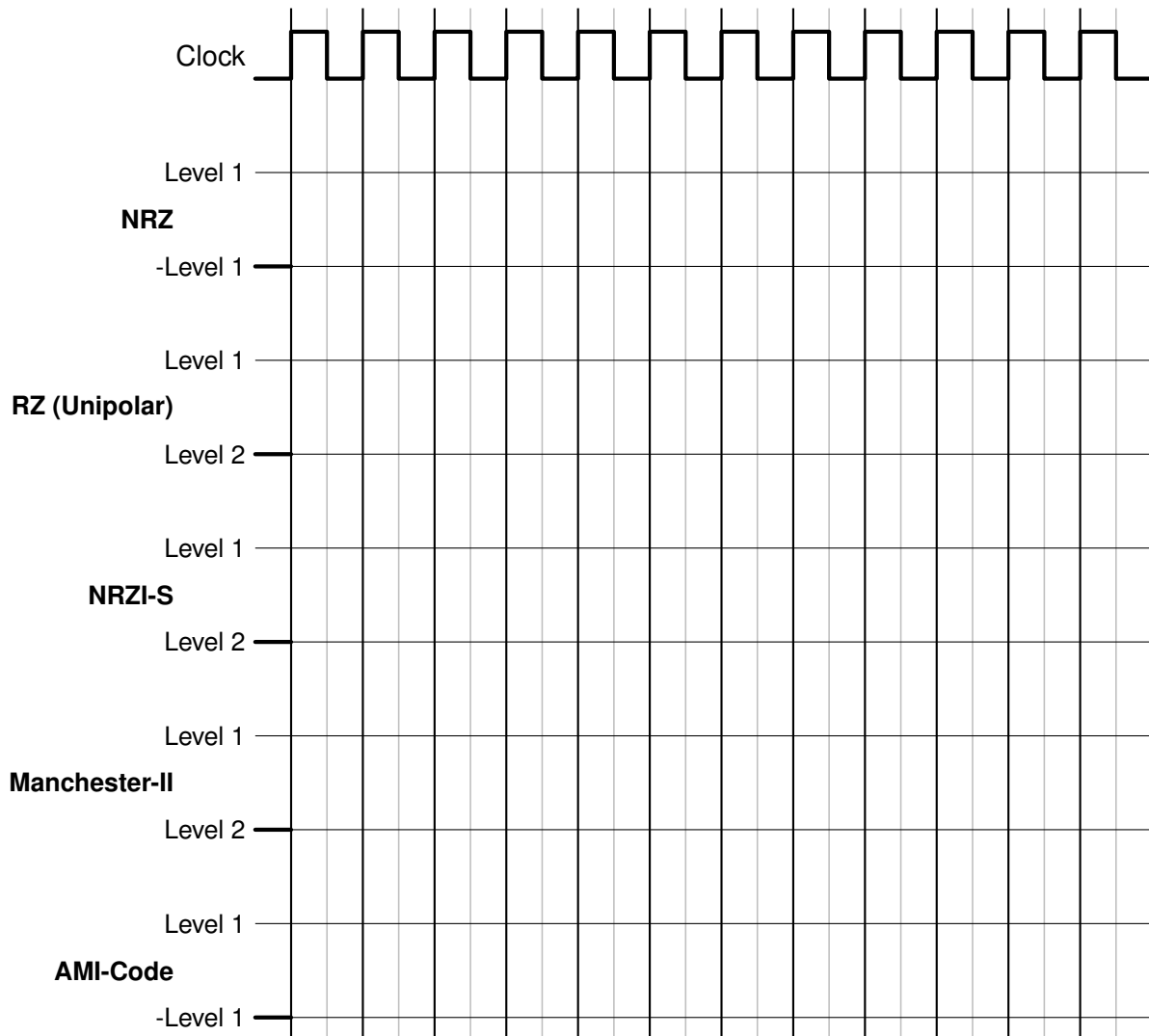


Figure 2.1: Line codes

2.2 Classify the following line codes according to their clock recovery properties for three possible different inputs, a long sequence of '1's, a long sequence of '0's, and an unknown signal. Mark in the table with a 'yes' or 'no' if the code enables the recovery of the clock for the specific input.

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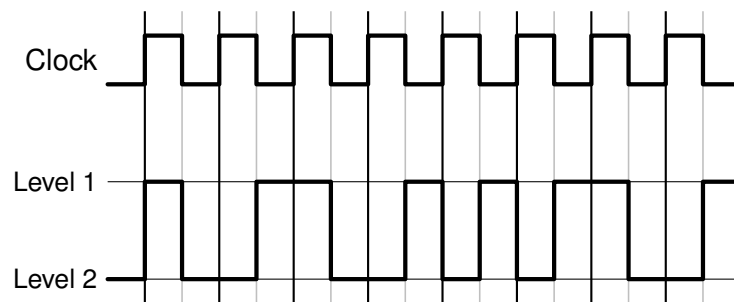
Code \ Input	'1's	'0's	unknown
RZ (Unipolar)			
NRZI-S			
Manchester-II			
AMI-Code			

2.3 What Line code has been used to encode the Data Sequence **1010 0010** below?

Under what condition does no DC component exist for the code?

In addition, briefly explain one problem that may arise from a non DC balanced code.

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Asynchronous Transmissions

2.4 An approach used to synchronize communication processes is Flow Control. Complete the signals in Figure 2.2 to perform two new transmissions with the DATA values 0xA and 0xB using *Level-Triggered Closed-loop Flow Control II*. Ignore delays and consider that:

- the Sender samples and sets signals with the rising edge of CLK_S .
- the Receiver samples and sets signals with the rising edge of CLK_R .
- the Sender and Receiver will set or unset their signals as soon as possible.
- the Receiver requires one clock cycle to consume the incoming data.
- at $t = 0$ ns, BUSY and VALID are '0' and DATA is undefined.

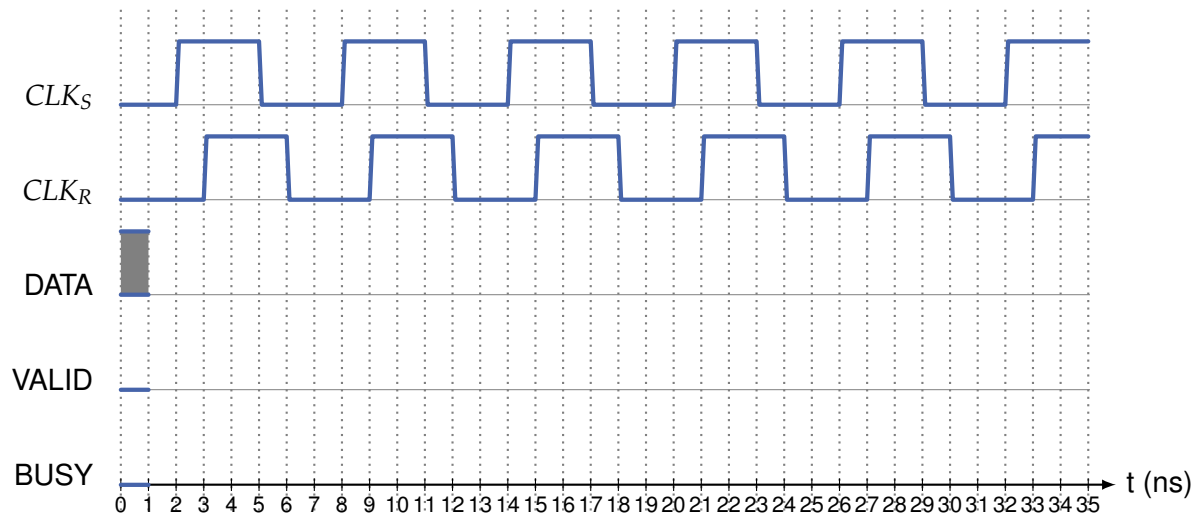


Figure 2.2: Signal sequence

2.5 Give one disadvantage that can occur when using Level-Triggered Closed-Loop Flow Control II? Explain briefly.

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2.6 **Start-Stop-mode** is a common synchronisation scheme used in serial asynchronous transmissions. Figure 2.3 presents a serial signal where a value was transmitted using a **7E1** Start-Stop mode (7 data bits, Even parity, 1 Stop bit).

What is the binary value of the data transmitted in this signal? Write it in the space given below. Additionally, identify Start, Stop, Parity, Idle and Data Value fields. Write the name of the fields clearly using the space available in the diagram above the signal. Assume that CLK_R is the receiver clock used to sample the incoming signal at the rising edge of the clock.

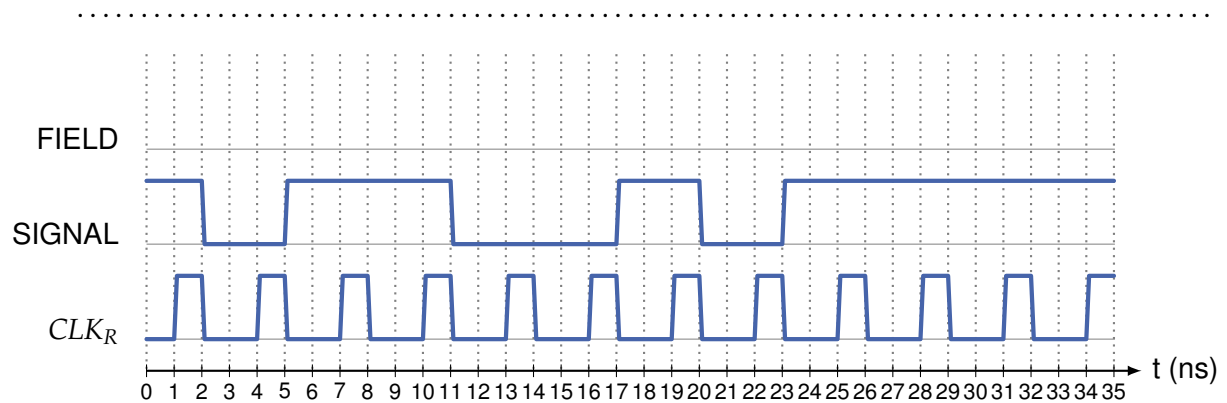


Figure 2.3: Signal sequence with Start-Stop mode

Is the transmitted data error free? Justify your answer.

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Task 3: Modulation

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Basic Questions

Table 3.1 shows four modulated signals.

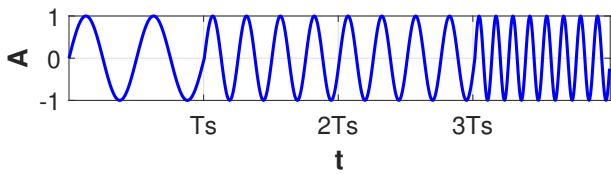
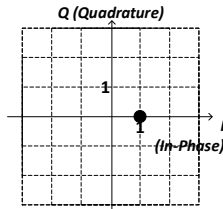
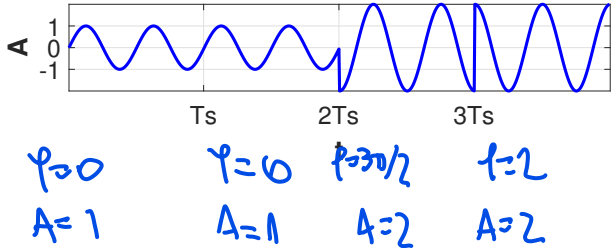
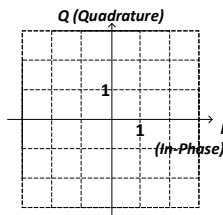
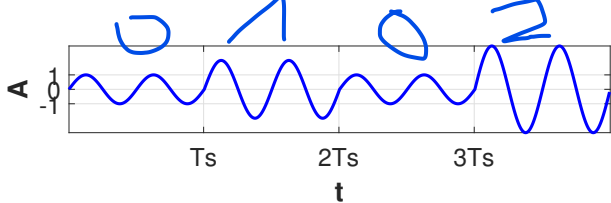
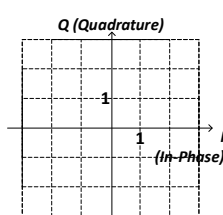
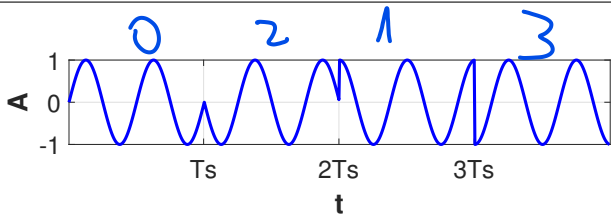
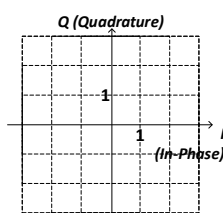
1: Signal	2: Name	3: Constellation Diagram	4: Symbols
	FSK		0,1,1,2
	QAM		
	ASK		
	PSK		0,2,1,3

Table 3.1: Modulated signals

3.1 Fill column 2 in Table 3.1 with the modulation names of each modulation. The first row is given as an example.

Hint: Give the most specific modulation, i.e. QAM is only a valid solution if none of the other modulations fit.

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3.2 Fill column 3 in Table 3.1 with the constellation diagram of each modulated signal. The first symbol (leftmost in the waveform) should have phase 0. The first row is given as an example.

Hint: Only add symbols which are actually used in the waveform. Do not include symbols only for symmetry reasons.

3.3 Fill column 4 in Table 3.1 with the symbols that were modulated in each modulated signal. Assign increasing numbers to symbols in the order as first seen from left to right in the waveform. The first row is given as an example.

Quadrature Amplitude Modulation

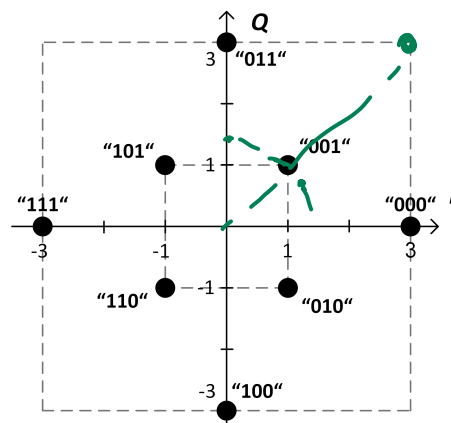
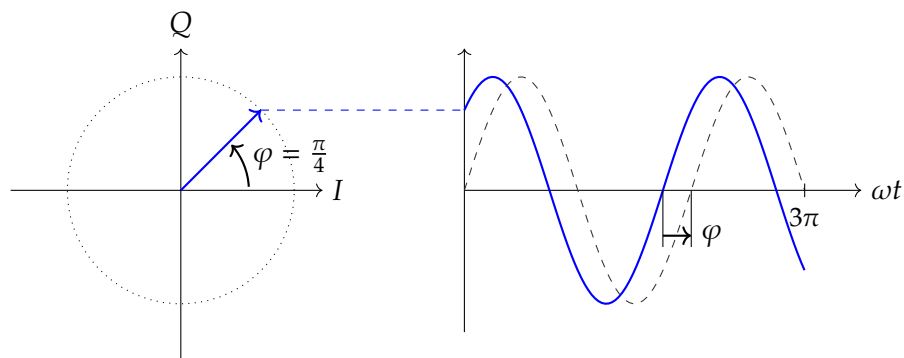


Figure 3.1: QAM constellation diagram

Figure 3.2: Definition of the phase difference of a sine signal compared to a reference signal (dashed line $\hat{=}$ reference signal).

3.4 The symbol constellation from Figure 3.1 is used by a transmitter to modulate data bits on a carrier. The phase φ of the signal is defined relative to a sine reference signal as shown in Figure 3.2. The modulated signal is shown in Figure 3.3, where T_s is the symbol period. Demodulate the signal and write down the resulting bit-stream.

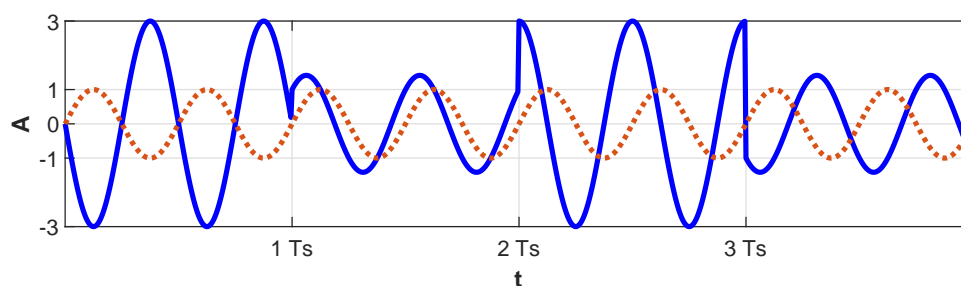


Figure 3.3: QAM modulated signal

Binary Data:

3.5 A signal is modulated with the constellation diagram from Figure 3.4 and transmitted on a coaxial cable. The sender is able to generate a maximum voltage amplitude U_{max} of ± 10 V, the receiver can accept larger voltages.

- Calculate the largest possible acceptance radius r_a for the symbols in the constellation diagram, keeping the relative distances between symbols as in Figure 3.4.
- Draw the acceptance radius around each symbol in Figure 3.4.

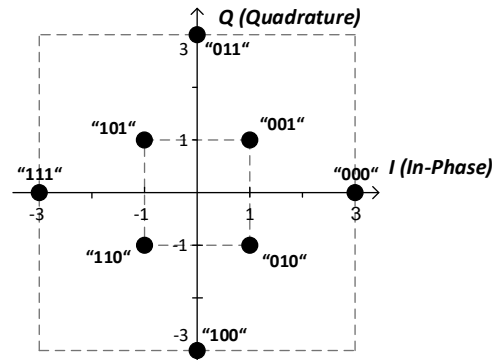


Figure 3.4: QAM constellation diagram: Acceptance radius

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3.6 Reconsider the constellation diagram from Figure 3.4. Assume that r_a is 1 V, the maximum voltage of the sender is 3 V and the symbols are as given in the figure. Can additional symbols be added without changing any of the previously mentioned parameters? Explain your answer.

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3.7 Explain what the acceptance radius is used for and why it is needed.

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- 3.8 Assume some data has been transmitted using the constellation diagram from Figure 3.5 on a noisy channel. All received noisy samples have a maximum deviation of amplitude of 1. Depict the noise in Figure 3.5 by drawing at least 5 noisy samples each for the symbols 001 and 100 into the diagram.

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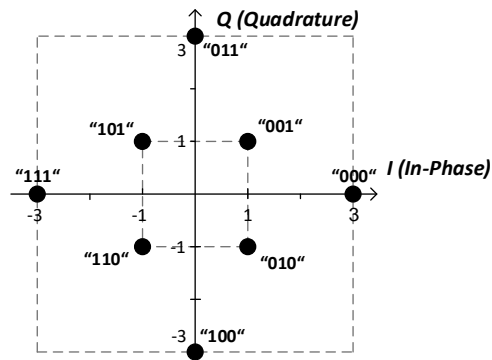


Figure 3.5: QAM constellation diagram: Noise

- 3.9 If the acceptance radius and location of symbols in the constellation diagram is given, what other aspect related to symbol encoding should be considered to reduce bit errors?

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Multiplexing

3.10 What is multiplexing used for?

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3.11 Name and shortly explain 2 multiplexing techniques which are not CDMA.

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Sender Node	Function							
n_0	+1	+1	+1	+1	+1	+1	+1	+1
n_1	+1	-1	+1	-1	+1	-1	+1	-1
n_2	+1	+1	-1	-1	+1	+1	-1	-1

Table 3.2: Walsh functions for nodes

3.12 Table 3.2 shows 3 codes which shall be used for CDMA. What property do these codes have to fulfill to be usable in CDMA schemes?

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3.13 Prove that the codes in Table 3.2 can be used for CDMA. For each individual calculation, provide the approach with variables, **one** step with concrete numbers inserted and the solution.

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3.14 Find a fourth Walsh function which is orthogonal to the three Walsh functions in Table 3.3.

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Sender Node	Function			
n_0	+1	-1	+1	-1
n_1	-1	-1	-1	-1
n_2	+1	-1	-1	+1
n_3				

Table 3.3: Only three Walsh functions, but we need four.

Task 4: Media Access

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General questions

4.1 Name two advantages of CSMA/CD in contrast to Aloha. Explain your answers briefly.

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4.2 Arrange the media access schemes CSMA/CR, CSMA/CD and Aloha according to their average channel utilization, start with the lowest channel utilization.

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4.3 CSMA (P-persistent Scheme) is used as transmission scheme. For each transmit request the channel is checked to be free. Briefly describe the behaviour of a node that wants to send data.

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4.4 CSMA/CD is used as transmission scheme. Is the length of the media related to the duration of sending? Give a short explanation.

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4.5 How does CSMA/CD react to a collision? Briefly describe the behaviour of a sending node until the message is successfully sent.

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Carrier Sense Multiple Access/Collision Resolution

A bus system of four nodes is using CSMA/CR as arbitration scheme and is connected via open collector drivers and a wired-AND connection. Each node has a five Bit identifier and the bus has to cover a maximum distance of 600m.

- 4.6 Which requirement has to be fulfilled in order to guarantee a faultless function of the system? What are the implications for the transmission rate?

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- 4.7 The data format uses a frame with a Start Of Frame bit (SOF) and an identifier with five bits. 4.1 shows an impulse diagram for the bus system described above and the signal level of the shared bus line. Indicate the identifiers of the given nodes as far as possible (use Table 4.1, mark uncertain identifier bits as X). Which node is granted exclusive access to the bus?

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node	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4
A					
B					
C					
D					

Table 4.1: Identifiers of the nodes

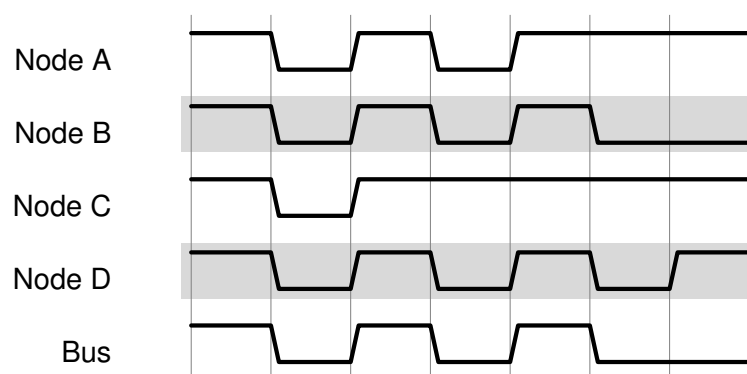


Figure 4.1: Bus Access

Arbitration

- 4.8 Name one advantage of arbitration compared to static multiplexing schemes like TDMA. Justify your answer briefly.

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- 4.9 Explain the differences between centralized and decentralized arbitration schemes briefly.

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- 4.10 Name two benefits of the arbitration scheme Tap Line. Justify your answer briefly.

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- 4.11 A system using Tapline is shown in Figure 4.2. An exemplary arbitration cycle of the system is shown in Figure 4.3. The prioritization is defined as follows: Node 0 > Node 2 > Node 1 > Node 3. The transmission is ongoing and at the time t_0 node 1 and node 2 want to send data. At time t_1 node 3 wants to send data. The sending time for all data packages of all senders are equal. The time steps are shown at the top of the Figure 4.3, complete this diagram accordingly. Mark down the sending nodes and the signal curves of each signal line.

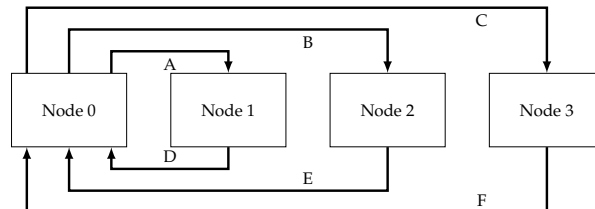


Figure 4.2: Tap Line

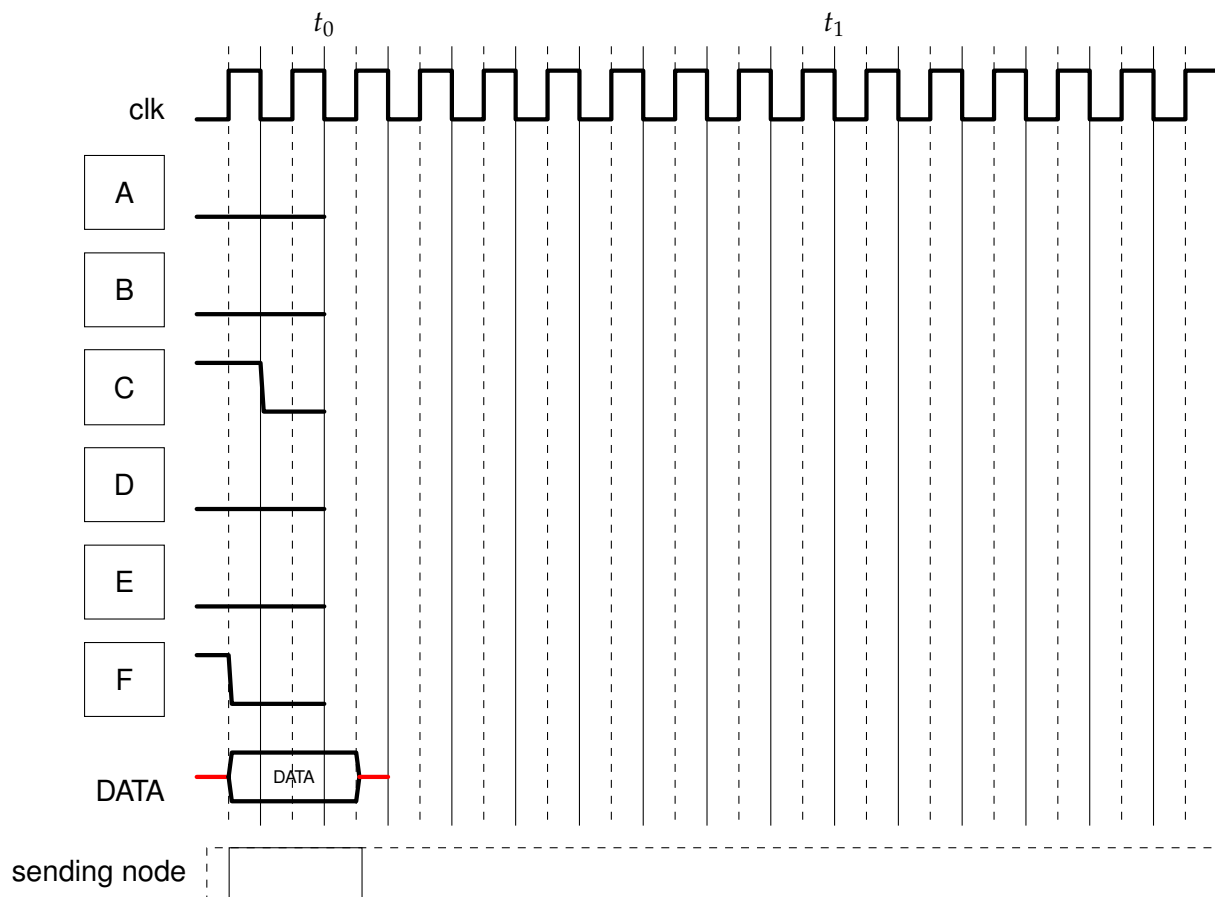


Figure 4.3: Signal flow for Tap Line

Task 5: Error Protection

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Cyclic Redundancy Check (CRC)

- 5.1 Does the CRC scheme based on the generator polynomial $G(x) = (x + 1)(x^2 + 1)$ allow a receiver to detect all error patterns with exactly three erroneous bits? Justify.

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- 5.2 The receiver of a CRC-protected message performs the CRC error detection procedure and calculates a non-zero remainder. What can it reliably conclude with respect to the occurrence of a transmission error?

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- 5.3 Two nodes use the generator polynomial $G(x) = x^4 + x + 1$ to exchange CRC-protected messages. To transmit a certain message, the sender calculates the corresponding checksum, appends this checksum to the raw message, and finally transmits the bit string

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0010 1110 1010 0011.

Due to transmission errors, however, the recipient receives the bit string

0010 1000 0010 0011.

Is the receiver, who is aware of $G(x)$, able to detect this error? Justify your answer based on the error pattern and the specific error detection capabilities of $G(x)$.

Hint: Do not perform the calculation that the receiver has to perform to detect errors!

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- 5.4 Given the generator polynomial $G(x) = x^5 + x^4 + 1$, what calculation does the receiver of the CRC-protected bit string "1111 0110 0001" perform as part of its error detection procedure? Give both the dividend and the divisor of this calculation as a bit string.

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Hint: This question does not require you to perform the calculation!

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5.5 To transmit it over a channel, the message “0100 0111 01” shall be protected by a CRC checksum. Using the generator polynomial $G(x) = x^4 + x^3 + x + 1$, calculate this checksum and give the bit string that is sent to the receiver.

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This image shows a full page of blank graph paper. The grid consists of small, uniform squares formed by thin, light gray lines. There are no margins, text, or other markings on the page.

5.6 Give the CRC generator polynomial that is implemented by the linear feedback shift register shown in Figure 5.1.

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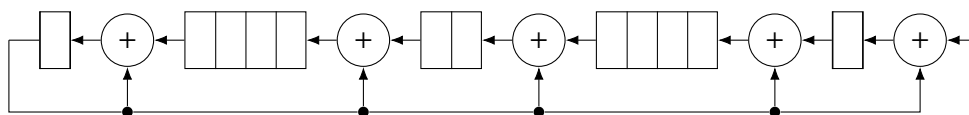


Figure 5.1: Simplified shift register implementation of a CRC scheme

Controller Area Network (CAN)

5.7 Consider a CAN network that consists of three individual CAN nodes. One of these nodes, in the following referred to as the sender, transmits a data frame that is received by the remaining two nodes (see Figure 5.3). While the CRC field is transmitted, receiver 1 reads an incorrect value from the bus and, therefore, does not acknowledge the reception of the data frame in the ACK field. Complete the empty columns in Figure 5.3 with the signal values that the three CAN nodes transmit in response to this event and determine the resulting bus level for all columns.

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Hint: Initially, all nodes are in the "error active" state. The general form of a CAN error frame is visualized in Figure 5.2. One column in Figure 5.3 corresponds to one bit duration.

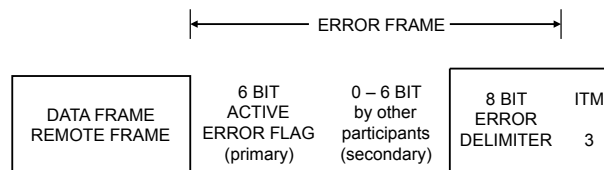


Figure 5.2: Error frame of the CAN protocol

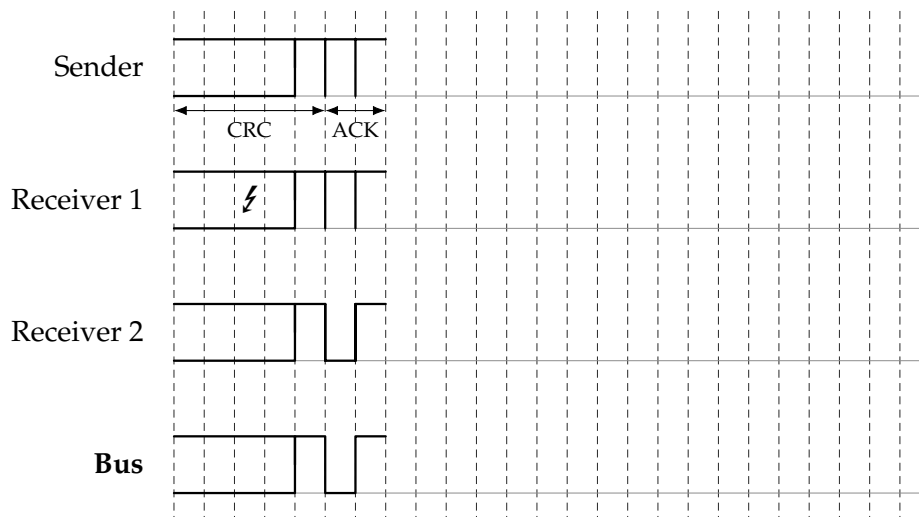


Figure 5.3: Signal sequence diagram of the CAN bus

5.8 Explain the bit monitoring rule from the CAN specification and describe how this mechanism is used for the purposes of error detection.

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5.9 Other than the bit monitoring rule mentioned in Task 5.8, name two error detection mechanisms incorporated into the CAN specification.

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5.10 How does the error frame transmitted by an “error active” node differ from the error frame transmitted by an “error passive” node? Give a brief explanation.

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Task 6: Protocols

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FireWire Arbitration

The result of the self-identify process for a FireWire network is shown in Figure 6.1. The number shown in the center of each node represents its physical ID given by the self-identify process.

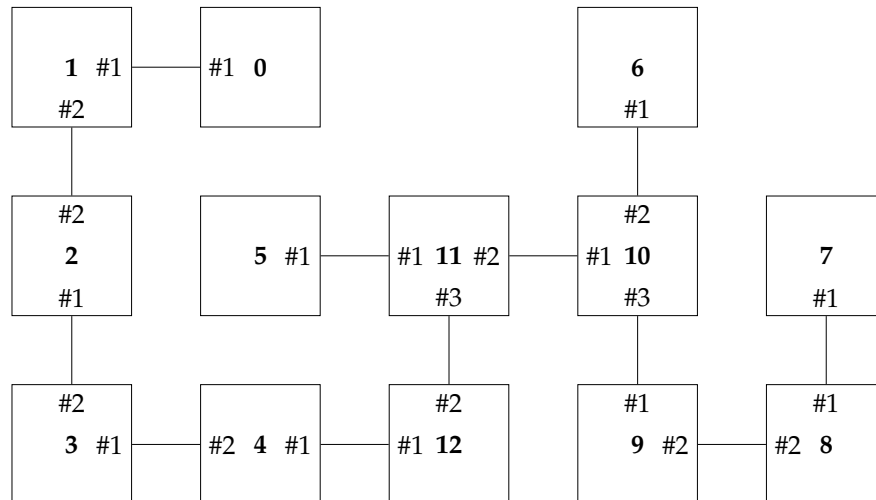


Figure 6.1: FireWire network

6.1 The nodes in Figure 6.1 having address 2, 5, 7, 10 would like to transmit data and start requesting at the same time. Describe in which order are the nodes granted request.

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- Assume that every node needs one time unit for processing and forwarding of its request signal.
- If a node receives multiple bus requests, it will always forward the request that it receives from the port with the lowest number.

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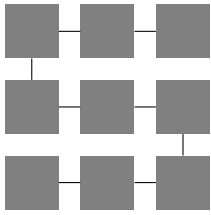
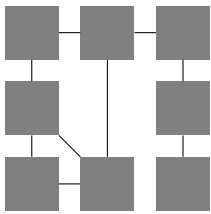
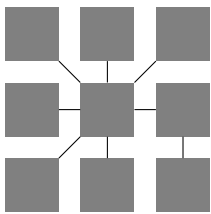
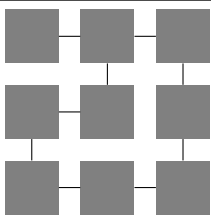
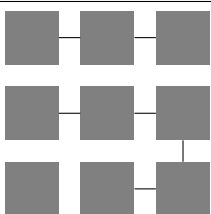
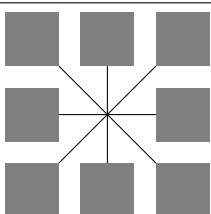
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FireWire Structures

6.2 Different FireWire structures were built, but not all of them are working correctly. State for each row if the nodes shown are building *one connected* FireWire system that is working correctly. If a system is correct, mark its root node. If it is not correct, give a reason for this.

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	Correct	Wrong	Reason
			
			
			
			
			
			

FireWire Architecture

6.3 Name the three stacked protocol layers of FireWire presented in the lecture.

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FireWire Encoding

6.4 Indicate the impulse diagram for the case that the following bit sequence (given in binary notation) should be transmitted: 010110010011_b. Use Figure 6.2.

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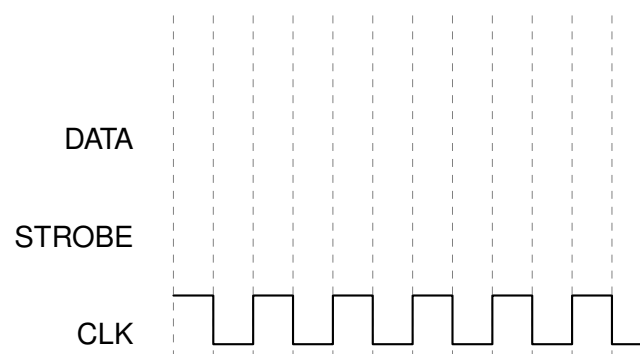


Figure 6.2: FireWire impulse diagram

Serial Peripheral Interface Bus (SPI)

The Serial Peripheral Interface bus (SPI) is a synchronous serial communication bus specification used for short distance communication.

The SPI bus specifies the following logic signals:

- **SCLK**: Serial Clock (output from master).
- **MOSI**: Master Output Slave Input (data output from master).
- **MISO**: Master Input Slave Output (data output from slave).
- **SS**: Slave Select (active low, output from master).

Consider the following protocol options and hints:

- The master selects each slave device with a logic level 0 on the individual select line.
- No waiting period between slave select low and first clock cycle.
- No waiting period between slave select high and last data transmission.
- Slave devices have tri-state outputs so their MISO signal becomes high impedance when the device is not selected.
- During each SPI clock cycle, a full duplex data transmission occurs between master and each slave device.

- 6.5 Draw the timing diagram for the case that the following data byte (given in binary notation) should be transmitted to a single slave: 01101011_b . As part of the transmission, the slave sends back the data byte: 00001101_b . Assume the data is captured on the rising edge of the clock and all slaves are unselected at the beginning. Use Figure 6.3.

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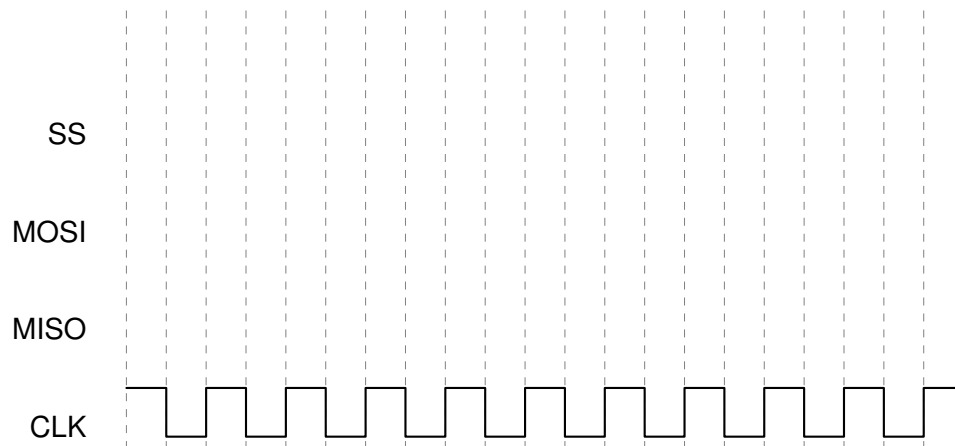


Figure 6.3: SPI full-duplex operation timing diagram

- 6.6 Figure 6.4 shows an SPI read operation of **1 byte** from a single slave. Add an appropriate SS signal to the diagram and write down the data the master **reads** from the slave in binary notation. Assume the data is captured on the rising edge of the clock and all slaves are unselected at the beginning.

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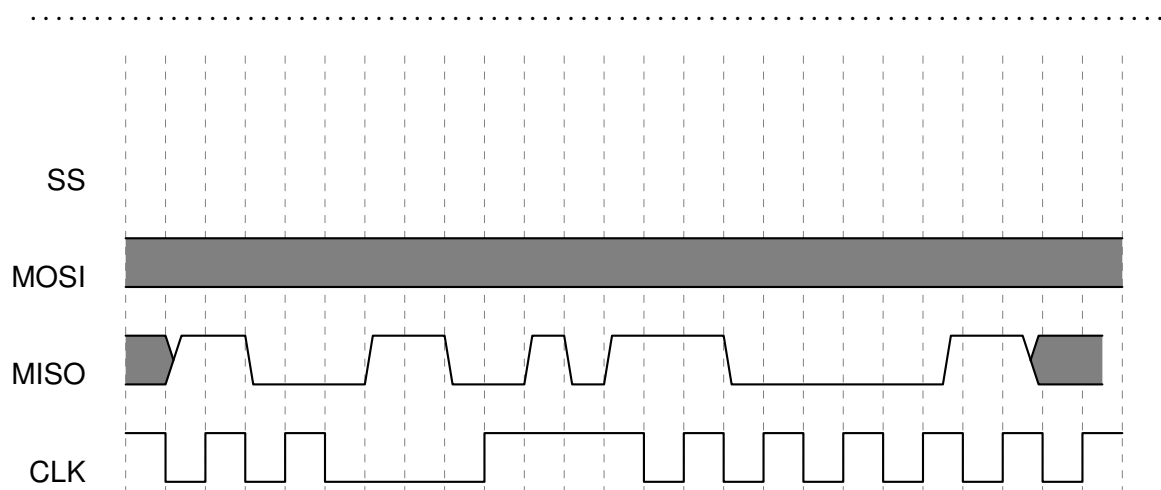


Figure 6.4: SPI read operation timing diagram

Task 7: Routing

/31

Switching

- 7.1 The switch matrix crossbars of a router can be implemented using full or reduced crossbars. Describe how both differ in terms of hardware resources and routing capabilities.

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- 7.2 One of the switching modes is *circuit switching*. Explain how the transmission of a message is handled using the different flit types.

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- 7.3 Name two advantages and two disadvantages of *circuit switching*.

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- 7.4 Imagine a network with a large link width (e.g. 16 bytes), allowing to fit entire messages within one single flit. Compare this network with another one with smaller link width of one byte. The clock frequency used on both are the same. Most of the messages transferred on both networks are of 10 bytes. Which switching scheme is better suited for which of these networks? Justify your decision.

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Routing

7.5 Name three optimization goals for a routing algorithm.

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7.6 Explain static and dynamic routing.

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7.7 Figure 7.1 shows a network topology with equal weights w_n on every link. Give the number of hops of the route from node A to F using *minimal routing*. In addition, describe how the number of hops from A to F could change if weights are differing and non-minimal routing is used.

/4

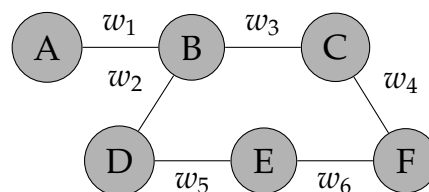


Figure 7.1: A network topology

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7.8 Figure 7.2 represents a network for which an optimal routing has to be found. The weights represent an abstract metric for traffic present at each connection. With node A as the starting point, calculate the paths with the lowest total traffic in the network by using Dijkstra's algorithm. Fill in Table 7.1 with the order in which nodes are visited in each step and the shortest paths after visiting the corresponding node.

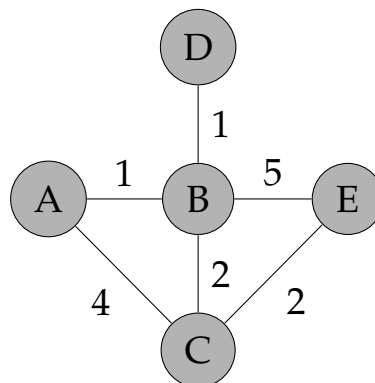


Figure 7.2: Given network topology

node	step 0		step 1		step 2		step 3		step 4		step 5	
	A											
vertex	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.	dist.	pred.
A	0	A										
B	∞	-										
C	∞	-										
D	∞	-										
E	∞	-										

Table 7.1: Dijkstra's algorithm

Task 8: Network-on-Chip

/31

General Questions

8.1 Define the edge connectivity of a network. What is the edge connectivity of a 3x7 torus network?

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8.2 Name the three basic building blocks in a Network-on-Chip.

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8.3 Compute the edge connectivity and diameter for the following topologies. All links here are bidirectional. Answer this question by filling in the empty cells in Table 8.1.

/8

Topology	Edge Connectivity	Diameter
6x7 Mesh		
7 Node Star		
8 Node Ring		
3x3x4 Mesh		

Table 8.1: Topologies and Metrics

8.4 Explain deadlock in a network.

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8.5 Name one motivation for using virtual channels in a NoC router.

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Fault Tolerant Routing

A system which comprises of 25 Processing Tiles is designed. They are interconnected using a NoC and the topology used is a 5x5 mesh. Packet switching is used and XY routing is implemented in the routers.

- 8.6 Find the path of packets from the source $(x,y) = (0,3)$ to the destination $(x,y) = (3,2)$ using XY routing. In your answer please name all traversed nodes (i.e. their coordinates) in the correct sequence.

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Overtime, certain routers experienced failure. Router at $(2,3)$ stopped working due to internal failure and cannot accept packets anymore. The failed router is illustrated in Figure 8.2. To continue supporting communication between other working routers, XY routing at each router was replaced with a custom adaptive routing algorithm which follows the rules provided below.

- Rule1 Try to first route the packet in the X direction towards the destination. Then the Y direction towards the destination. If the link chosen leads to a failed router, do not select this link and go to Rule 2. If the link chosen leads to an already visited router, do not select this link and go to Rule 2.
- Rule2 Choose among the remaining directions in the decreasing order of priority $+y,-y,+x,-x$. Use Figure 8.1 as a guide. If the link chosen leads you to a failed router, do not select this link and repeat Rule 2. If the link chosen leads to an already visited router, do not select this link and repeat Rule 2. If there are no more links available, drop the packet.
- 8.7 What is the path a packet takes from the source $(x,y) = (1,3)$ to the destination $(x,y) = (2,2)$ using the custom adaptive routing described above? In your answer please name all traversed nodes (i.e. their coordinates) in the correct sequence. Mention which of the above mentioned rules you used to go to the next node.

/11

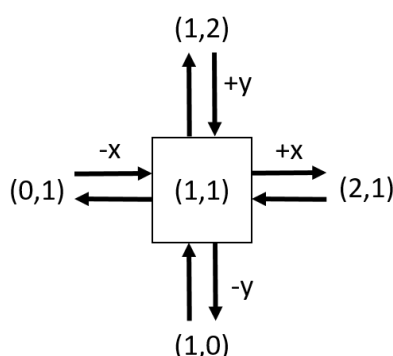


Figure 8.1: Node at $(x,y) = (1,1)$

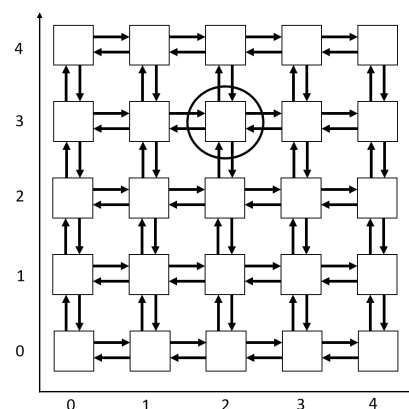


Figure 8.2: 5x5 Mesh network

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8.8 Define Minimal Routing. Is the custom adaptive routing used in the previous task minimal?

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Additional sheet for Task :